REMARKS

This paper is being provided in response to the Office Action mailed May 5, 2004, for the above-referenced application. In this response, Applicants have amended claims 1 and 17 to clarify that which Applicants consider to be the invention. Applicants respectfully submit that the amendments to the claims are fully supported by the originally-filed application.

Applicants thank the Examiner for the allowance of claim 24.

The rejection of claims 1-4, 6-7, 9, 17-19, 20 and 22-23 under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,229,368 to Lee (hereinafter "Lee") is hereby traversed and reconsideration is respectfully requested in view of the amendments to the claims contained herein.

Independent claim 1, as amended herein, recites a delay locked loop (DLL) circuit comprising a delay circuit which is connected to first and second nodes and which delays an original clock signal supplied to the first node based on a delay control signal. The delay circuit generates first to n-th (n is an integer more than 1) internal clock signals. The first internal clock signal is outputted from the second node. The internal clock signals other than the first internal clock signal are outputted from the delay circuit without passing through the second node and lead the first internal clock signal in phase by a predetermined phase value. The original clock signal is a frequency variable clock signal and the delay circuit includes a first delay section with a frequency dependent delay time based on the frequency variable clock signal and a second delay section with a fixed delay time independent of said frequency variable clock signal. A

phase comparing circuit compares the original clock signal and the first internal clock signal and outputs a phase difference. A delay control circuit outputs the delay control signal to the delay circuit based on the phase difference outputted from the phase comparing circuit. Further, a logic circuit generates a latch signal in synchronism with the first internal clock signal and generates an enable signal in synchronism with at least one of said internal clock signals other than said first internal clock signal. Claims 2-9 depend directly or indirectly on claim 1.

Independent claim 17, as amended herein, recites a method of generating timing signals, comprising delaying an original clock signal supplied to a first node based on a delay control signal. First to n-th (n is an integer more than 1) internal clock signals are generated from the delayed original clock signal. The first internal clock signal is outputted from a second node and the internal clock signals other than the first internal clock signal are outputted without passing through the second node and lead the first internal clock signal in phase by a predetermined value. The original clock signal is a frequency variable clock signal, and a first delay section with a frequency dependent delay time based on the frequency variable clock signal and a second delay section with a fixed delay time independent of the frequency variable clock signal control delay of the original clock signal and the internal clock signals. A phase difference between the original clock signal and the first internal clock signal is detected. The delay control signal is generated based on the detected phase difference. Further, the method includes generating a latch signal in synchronism with the first internal clock signal and generating an enable signal in synchronism with at least one of said internal clock signals other than said first internal clock signal. Claims 18-23 depend directly or indirectly on independent claim 17.

The Lee reference discloses internal clock generating circuits having delay compensation. Lee discloses a DLL circuit 111 that includes a phase detector 111a, a delay control circuit 111d, a delay line 111b and a clock signal buffer 111c. The delay control circuit 111d controls the delay time of the delay line 111b in response to the output of the phase detector 111a. (See Figure 1, and col. 7, lines 1-5 of Lee.)

Applicants' independent claims 1 and 17 recite a DLL circuit and a method of generating timing signals that includes generating a latch signal in synchronism with the first internal clock signal and generating an enable signal in synchronism with at least one of said internal clock signals other than said first internal clock signal. Applicants respectfully submit that Lee does not teach or fairly suggest at least the above-noted features as claimed by Applicants. Accordingly, Applicants respectfully request that this rejection be reconsidered and withdrawn.

The rejection of claims 5, 8 and 21 under 35 U.S.C. 103(a) as being unpatentable over Lee is hereby traversed and reconsideration is respectfully requested in view of the amendments to the claims contained herein.

The features of independent claims 1 and 17 are discussed above with respect to the Lee reference. Claims 5, 8 and 21 depend thereon.

As noted above, Applicants respectfully submit that Lee does not teach or fairly suggest at least the features of a DLL circuit and a method of generating timing signals that includes generating a latch signal in synchronism with the first internal clock signal and generating an

enable signal in synchronism with at least one of said internal clock signals other than said first internal clock signal, as is claimed by Applicants. Accordingly, Applicants respectfully request that this rejection be reconsidered and withdrawn.

Based on the above, Applicants respectfully request that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-248-4038.

Respectfully submitted,
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